CLAIMS

1. Process for displaying data on a matrix display consisting of N data lines and P selection lines at the intersections of which are situated the image points or pixels, and in which the N data lines are grouped into P' blocks of N' data lines each (N = P × N'), each block receiving in parallel one of the P' data signals which is demultiplexed on the N' lines of the said block, characterized in that, alternately according to the selection lines, the scanning of the N' data lines of a block is carried out from 1 to N' or from N' to 1.

2. Process according to Claim 1, characterized in that the scan from 1 to N' then from N' to 1 is carried out every second selection line.

3. Process according to Claim 1, characterized in that the scan from 1 to N' then from N' to 1 is carried out for four successive selection lines, the scan being carried out in a first direction for two successive selection lines and in a second direction for the other two succeeding selection lines.

4. Circuit for implementing the process according to any one of Claims 1 to 3, characterized in that it consists of at least one programmable logic circuit associated with a line counter determining the reversal of the direction of scan.